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TITLE: RAM testing device

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PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 421955 B	March 11, 2004	N/A	000	G11C 029/00
KR 2003018996 A	March 6, 2003	N/A	001	G11C 029/00

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR 421955B	N/A	2001KR-0053619	August 31, 2001
KR 421955B	Previous Publ.	KR2003018996	N/A
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BASIC-ABSTRACT:

NOVELTY - A RAM testing device is provided, which is capable of judging an error state of a RAM exactly so as to improve an error testing property by inputting test data generated with a simple circuit to the RAM and testing the RAM according to an input result.

DETAILED DESCRIPTION - A test signal generating part(2) generates and output a pseudo-random bit sequence(PRBS) pattern signal for detecting an error of a RAM(1). An address generating part(3) adds an input address signal to the pattern signal and generates an output address signal delayed by one address selected from outputs of the RAM. A RAM control signal generating part(4) generates control signals of the RAM in synchronization with an

address signal of the address generating part(3). A comparator(5) compares an input test signal of the test signal generating part and a pattern signal of the RAM loaded on an output address signal of the output address signal of the address generating part(3) and outputs an operation error judgment signal of the RAM.

CHOSEN-DRAWING: Dwg.1/10
TITLE-TERMS: RAM TEST DEVICE

DERWENT-CLASS: S01 U11 U14

EPI-CODES: S01-G01A1; U11-F01C5; U11-F01D2B; U14-D;